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Attorney's Docket No.: 42P8931C

Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:
Sujat Jamil et al.

Examiner: Verbrugge, K.

Application No. 10/620,629

Art Unit: 2188

Filed: July 15, 2003

CERTIFICATE OF TRANSMISSION

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Lawrence Mennemeier

Assistant Commissioner for Patents
Washington, D.C. 20231

INFORMATION DISCLOSURE STATEMENT

Sir:

Enclosed is a copy of Information Disclosure Citation Form PTO-1449
together with copies of the documents cited on that form. It is respectfully
requested that the cited documents be considered and that the enclosed copy of
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indicate such consideration and a copy thereof returned to applicant(s).

Pursuant to 37 C.F.R. § 1.97, the submission of this Information Disclosure Statement is not to be construed as a representation that a search has been made and is not to be construed as an admission that the information cited in this statement is material to patentability.

Pursuant to 37 C.F.R. § 1.97, this Information Disclosure Statement is being submitted under one of the following (as indicated by an "X" to the left of the appropriate paragraph):


- X 37 C.F.R. §1.97(b).
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- A statement pursuant to 37 C.F.R. §1.97(e) or
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- (1) A statement pursuant to 37 C.F.R. §1.97(e);
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If there are any additional charges, please charge Deposit Account No.
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Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 11-30-04


Lawrence M. Mennemeier
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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 042P8931C	Application Number: 10/620,629
Sheet 2 of 4		First Named Inventor: Sujat Jamil	Examiner Verbrugge, K.
		Filing Date: July 15, 2003	Art Unit: 2188
OTHER ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
	A08	AGARWAL, A., et al., "The MIT Alewife Machine: A Large-Scale Distributed-memory Multiprocessor," <i>Technical Report MIT/LCS Memo TM-454, Laboratory for Computer Science, Massachusetts Institute of Technology</i> , 1991.	
	A19	ANDERSON, C., et al., "A Multi-Level Hierarchical Cache Coherence Protocol for Multiprocessors," <i>University of Washington</i> , 1992, 92-10-04	
	A18	ANDERSON, C., et al., "Design and Evaluation of a Subblock Cache Coherence Protocol for Bus-Based Multiprocessors," <i>University of Washington</i> , 1994, 94-05-02	
	A09	BIANCHI, R., et al., "Memory Contention in Scalable Cache-coherent Multiprocessors," <i>Technical Report 448, Computer Science Department, University of Rochester</i> , 1993.	
	B01	CENSIER, L.M., et al., "A New Solution to Coherence Problems in Multicache Systems," <i>IEEE Transactions on Computers</i> , Vol. C-27, No. 12, December, 1978, 7 pages	
	A20	CHAIKEN, D., et al., "LimitLESS Directories: A Scalable Cache Coherence Scheme," <i>Proceedings of the 4th Int'l Conference on ASPLOS</i> , pages 224-234, New York, April 1991.	
	A22	EGGERS, S.J., et al., "A Characterization of Sharing in Parallel Programs and Its Application to Coherency Protocol Evaluation," <i>Proceedings of the 15th Annual International Symposium on Computer Architecture</i> , May 1988.	
	A10	FARKAS, K., "Cache Consistency in Hierarchical-ring-based Multiprocessors," <i>Technical Report CSRI-273, Computer Systems Research Institute, University of Toronto, Ontario, Canada</i> , January 1993.	
	A11	FLEISCH, B., "A Coherent Distributed Shared Memory Design," <i>Proceedings from the 14th ACM Symposium on Operating System Principles</i> , pages 211-223, New York, 1989.	

Examiner Signature		Date Considered	
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*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication.

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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 042P8931C	Application Number: 10/620,629
Sheet 3 of 4	First Named Inventor: Sujat Jamil	Examiner Verbrugge, K.
	Filing Date: July 15, 2003	Art Unit: 2188

OTHER ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
	A06	GHARACHORLOO, K., et al., "Memory Consistency and Event Ordering in Scalable Shared-Memory Multiprocessors," <i>Proceedings of the 17th International Symposium on Computer Architecture</i> , pages 15-26, May 1990.	
	A05	GHARACHORLOO, K., et al., "Performance Evaluation of Memory Consistency Models for Shared-Memory Multiprocessors," <i>Proceedings of Fourth International Conference on Architectural Support for Programming Languages and Operating Systems</i> , pages 245-257, 1991.	
	A03	IEEE Std 1596-1992. "Scalable Coherent Interface," Piscataway, NJ.	
	A04	JOHNSON, R.E., "Extending the Scalable Coherent Interface for Large-Scale Shared-Memory Multiprocessors," <i>PhD Thesis, University of Wisconsin-Madison</i> , 1993.	
	A23	LENOSKI, D., et al., "The Directory-based Cache Coherence Protocol for the Dash Multiprocessor," <i>Proceedings of the 17th Int'l Symposium on Computer Architecture</i> , Los Alamitos, Calif., May 1990.	
	A13	LI, K., et al., "Memory Coherence in Shared Virtual Memory Systems," <i>ACM Transactions On Computer Systems</i> , 7(4):321-359, November 1989.	
	A14	LI, Q., et al., "Redundant Linked List based Cache Coherence Protocol," <i>World Computer Congress, IFIP Congress</i> , 1994.	
	A01	LILJA, D. J., "Cache Coherence in Large-Scale Shared-Memory Multiprocessors: Issues and Comparisons", <i>ACM Computing Surveys</i> , 25(3), September 1993	
	A15	MELLOR-CRUMMEY, J.M., et al., "Algorithms for Scalable Synchronization on Shared-memory Multiprocessors," <i>ACM Transactions on Computer Systems</i> , 9(1), Feb 1991.	
	A12	MORI, S., et al., "A Distributed Shared Memory Multiprocessor: ASURA - Memory and Cache Architectures," <i>Supercomputing '93</i> , pages 740-749, Portland, Oregon, November 1993.	

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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)		Attorney Docket No.: 042P8931C	Application Number: 10/620,629
Sheet 4 of 4		First Named Inventor: Sujat Jamil	Examiner Verbrugge, K.
		Filing Date: July 15, 2003	Art Unit: 2188
OTHER ART – NON PATENT LITERATURE DOCUMENTS			
	A16	NILSSON, H., et al., "The Scalable Tree Protocol - a Cache Coherence Approach to Large-scale Multiprocessors," <i>Proceedings of the 4th IEEE Symposium on Parallel and Distributed Processing</i> , May 1992.	
	A24	NITZBERG, B., et al., "Distributed Shared Memory: A Survey of Issues and Algorithms," <i>IEEE Computer</i> , pages 52-60, August 1991.	
	A02	PAPAMARCOS, M., et al., "A Low-Overhead Coherence Solution for Multiprocessors with Private Cache Memories," <i>Proc. 11th ISCA</i> , 1984, pp. 348-354.	
	B03	PCT International Search Report, PCT/US01/30359, mailed 10/08/2002, 5 pages	
	B02	PONG, F., et al., "Correctness of a Directory-Based Cache Coherence Protocol: Early Experience," <i>IEEE</i> , 1993, pp. 37-44	
	A21	SANDHU, H.S., et al., "The Shared Regions Approach to Software Cache Coherence on Multiprocessors," <i>Proceedings of the 4th ACM SIGPLAN Symposium on Principles and Practice of Parallel Programming</i> , May 1993.	
	A07	SCHEURICH, C., et al., "Correct Memory Operation of Cache-Based Multiprocessors," <i>Proceedings 14th Annual International Symposium on Computer Architecture</i> , pages 234-243, Pittsburgh, PA, June 1987.	
	A25	STUMM, M., et al., "Algorithms Implementing Distributed Shared Memory," <i>Computer</i> , 23(5):54-64, May 1990.	
	A17	TANG, C.K., "Cache System Design in the Tightly Coupled Multiprocessor System," <i>AFIPS Proceedings of the National Computer Conference</i> , 1976.	
	A27	THAKKAR, S., et al., "Scalable Shared-Memory Multiprocessor Architectures," <i>IEEE Computer</i> , 23(6), June 1990.	
	A26	THAPAR, M., et al., "Stanford Distributed Directory Protocol," <i>IEEE Computer</i> , pages 78-80, June 1990.	
	C01	Patent Act 1977: Examination Report under section 18(3), Application No: GB0309110.5 (International App. No. PCT/US01/30359), July 7, 2004	


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Form PTO-1449 (Modified)		Atty Docket No.: 042390.P8831		Serial No.: 09/677,122			
List of Patents and Publications Statement (Use several sheets if necessary) Page 1 of 2				Applicant: Sujat Jamil, et al.			
				Filing Date: 09/29/2000			
REFERENCE DESIGNATION				U.S. PATENT DOCUMENTS			
Examiner Initials		Document No.		Class	Sub- Class	Filing date if appropriate	
	AA						
	AB						
	AC						
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FOREIGN PATENT DOCUMENTS							
No.		Document No.	Date	Country	Class	Sub-Class	Trans- lation
	AQ						
	AR						
	AS						
	AT						
	AU						
OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)							
KU	A01	Lilja, D. J.. Cache Coherence in Large-Scale Shared-Memory Multiprocessors: Issues and Comparisons, ACM Computing Surveys, 25(3), September 1993					
KU	A02	M. Papamarcos and J. Patel, "A Low-Overhead Coherence Solution for Multiprocessors with Private Cache Memories," Proc. 11th ISCA, 1984 pp. 348-354.					
KU	A03	IEEE Std 1596-1992. Scalable Coherent Interface. Piscataway, NJ.					
KU	A04	R.E. Johnson. Extending the Scalable Coherent Interface for Large-Scale Shared-Memory Multiprocessors. PhD thesis, University of Wisconsin-Madison, 1993.					
KU	A05	Kourosh Gharachorloo, Anoop Gupta, and John Hennessy. Performance Evaluation of Memory Consistency Models for Shared-Memory Multiprocessors. In <i>Proceedings of Fourth International Conference on Architectural Support for Programming Languages and Operating Systems</i> , pages 245-257, 1991.					
KU	A06	Kourosh Gharachorloo, Daniel Lenoski, James Laudon, Phillip Gibbons, Anoop Gupta, and John Hennessy. Memory Consistency and Event Ordering in Scalable Shared-Memory Multiprocessors. In <i>Proceedings of the 17th International Symposium on Computer Architecture</i> , pages 15-26, May 1990.					
KU	A07	Christoph Scheurich and Michel Dubois. Correct Memory Operation of Cache-Based Multiprocessors. In <i>Proceedings 14th Annual International Symposium on Computer Architecture</i> , pages 234-243, Pittsburgh, PA, June 1987.					

<div style="text-align: center;">  </div>	<i>KW</i>	A08	A. Agarwal, D. Chaiken, G. D'Souza, et al. The MIT Alewife machine: A large-scale distributed-memory multiprocessor. Technical Report MIT/LCS Memo TM-454, Laboratory for Computer Science, Massachusetts Institute of Technology, 1991.	
	<i>KW</i>	A09	R. Bianchini, M. E. Crovella, L. Kontothanassis, and T. J. LeBlanc. Memory contention in scalable cache-coherent multiprocessors. Technical Report 448, Computer Science Department, University of Rochester, 1993. <i>Title Page missing</i>	
	<i>KW</i>	A10	K. Farkas, Z. Vranesic, and M. Stumm. Cache consistency in hierarchical-ring-based multiprocessors. Tech. Rep. CSRI-273, Computer Systems Research Institute, Univ. of Toronto, Ontario, Canada, January 1993.	
	<i>KW</i>	A11	B. Fleisch and G. Popek. Mirage: A coherent distributed shared memory design. In <i>Proceedings from the 14th ACM Symposium on Operating System Principles</i> , pages 211-223, New York, 1989.	
	<i>KW</i>	A12	S. Mori, H. Saito, M. Goshima, et al. A distributed shared memory multiprocessor: ASURA - memory and cache architectures -. In <i>Supercomputing '93</i> , pages 740-749, Portland, Oregon, November 1993.	
	<i>KW</i>	A13	K. Li and P. Hudak. Memory coherence in shared virtual memory systems. <i>ACM Transactions in Computer Systems</i> , 7(4):321-359, November 1989. RECE	
	<i>KW</i>	A14	Q. Li and S. Vlaovic. Redundant linked list based cache coherence protocol. In <i>World Computer Congress, IFIP Congress</i> , 1994. JAN 0	
	<i>KW</i>	A15	John M. Mellor-Crummey and Michael L. Scott. Algorithms for scalable synchronization on shared-memory multiprocessors. <i>ACM Trans. on Computer Systems</i> , 9(1), Feb 1991. Group	
	<i>KW</i>	A16	H. Nilsson and P. Stenstrom. The scalable tree protocol - a cache coherence approach to large-scale multiprocessors. In <i>Proceedings of the 4th IEEE Symposium on Parallel and Distributed Processing</i> , May 1992.	
	<i>KW</i>	A17	C.K. Tang. Cache system design in the tightly coupled multiprocessor system. In <i>AFIPS Proceedings of the National Computer Conference</i> , 1976.	
	<i>KW</i>	A18	Craig Anderson and Jean-Loup Baer. Design and Evaluation of a Subblock Cache Coherence Protocol for Bus-Based Multiprocessors. University of Washington, 1994, 94-05-02	
	<i>KW</i>	A19	Anderson, C. and J.-L. Baer. A Multi-Level Hierarchical Cache Coherence Protocol for Multiprocessors. University of Washington, 1992, 92-10-04	
	<i>KW</i>	A20	D. Chaiken, J. Kubiawicz, and A. Agarwal. LimitLESS directories: A scalable cache coherence scheme. In <i>Proc. of the Fourth Int'l Conf. on ASPLOS</i> , pages 224-234, New York, April 1991.	
	<i>KW</i>	A21	H. S. Sandhu, B. Gamsa, and S. Zhou. The shared regions approach to software cache coherence on multiprocessors. In <i>Proc. of the 4th ACM SIGPLAN Symp. on Principles and Practice of Parallel Programming</i> , May 1993.	
	<i>KW</i>	A22	S.J. Eggers and R.H. Katz. A characterization of sharing in parallel programs and its application to coherency protocol evaluation. In <i>Proceedings of the 15th Annual International Symposium on Computer Architecture</i> , May 1988.	
	<i>KW</i>	A23	D. Lenoski et al. The directory-based cache coherence protocol for the dash multiprocessor. In <i>Proc. 17th Int'l Symp. Computer Architecture</i> , Los Alamitos, Calif., May 1990.	
	<i>KW</i>	A24	Bill Nitzberg and Virginia Lo. Distributed shared memory: A survey of issues and algorithms. <i>IEEE Computer</i> , pages 52-60, August 1991.	
	<i>KW</i>	A25	M. Stumm and S. Zhou. Algorithms implementing distributed shared memory. <i>Computer</i> , 23(5):54-64, May 1990.	
	<i>KW</i>	A26	M. Thapar and B. Delagi. Stanford distributed directory protocol. <i>IEEE Computer</i> , pages 78-80, June 1990.	
	<i>KW</i>	A27	Shreekanth Thakkar, Michel Dubios, Anthony T. Laundrie, and Gurindar S. Sohi. Scalable Shared-Memory Multiprocessor Architectures. <i>IEEE Computer</i> , 23(6), June 1990.	
	Examiner <i>Kevin Verbruggen</i>		Date Considered <i>12/20/02</i>	
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

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Sheet 1 of 2

Complete if Known

Application Number	09/677,122
Filing Date	September 29, 2000
First Named Inventor	Sujat Jamil
Art Unit	2185 2158
Examiner Name	Keerthi Venk.
Attorney Docket Number	42390P8931

U.S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No.*	Foreign Patent Document Country Code* - Number* - Kind Code* (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
100	EP	0 397 994 A2	11-22-1990	International Business Machines Corporation	

**Examiner
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Substitute for form 1449A/PTO				Complete If Known	
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				Filing Date	September 29, 2000
				First Named Inventor	Sujat Jamil
				Art Unit	2185-2188
				Examiner Name	Kevin Verbrugge
Sheet	2	of	2	Attorney Docket Number	42390P8931

OTHER ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
KV	B01	CENSIER, L. M., et al., "A New Solution to Coherence Problems in Multicache Systems," IEEE Transactions on Computers, Vol. C-27, No. 12, December 1978, 7 pages.
KV	B02	PONG, F., et al., "Correctness of a Directory-Based Cache Coherence Protocol: Early Experience." IEEE, 1993, pgs. 37-44.
KV	B03	PCT International Search Report, PCT/US01/30359, mailed 10/08/2002, 5 pages.

Examiner Signature	<i>Kevin Verhege</i>	Date Considered	4/30/03
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